National Semiconductor

September 18, 2008

ADC10731/ADC10732/ADC10734/ADC10738 10-Bit Plus Sign Serial I/O A/D Converters with Mux, Sample/Hold and Reference

General Description

The ADC10731, ADC10732 and ADC10734 are obsolete or on lifetime buy and included for reference only.

This series of CMOS 10-bit plus sign successive approximation A/D converters features versatile analog input multiplexers, sample/hold and a 2.5V band-gap reference. The 1-, 2-, 4-, or 8-channel multiplexers can be software configured for single-ended or differential mode of operation.

An input sample/hold is implemented by a capacitive reference ladder and sampled-data comparator. This allows the analog input to vary during the A/D conversion cycle.

In the differential mode, valid outputs are obtained even when the negative inputs are greater than the positive because of the 10-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE serial data exchange standard for easy interface to the COPS and HPC families of controllers, and can easily interface with standard shift registers and microprocessors.

Features

- 0V to analog supply input range
- Serial I/O (MICROWIRE compatible)
- Software or hardware power down
- Analog input sample/hold function
- Ratiometric or absolute voltage referencing
- No zero or full scale adjustment required
- No missing codes over temperature
- TTL/CMOS input/output compatible

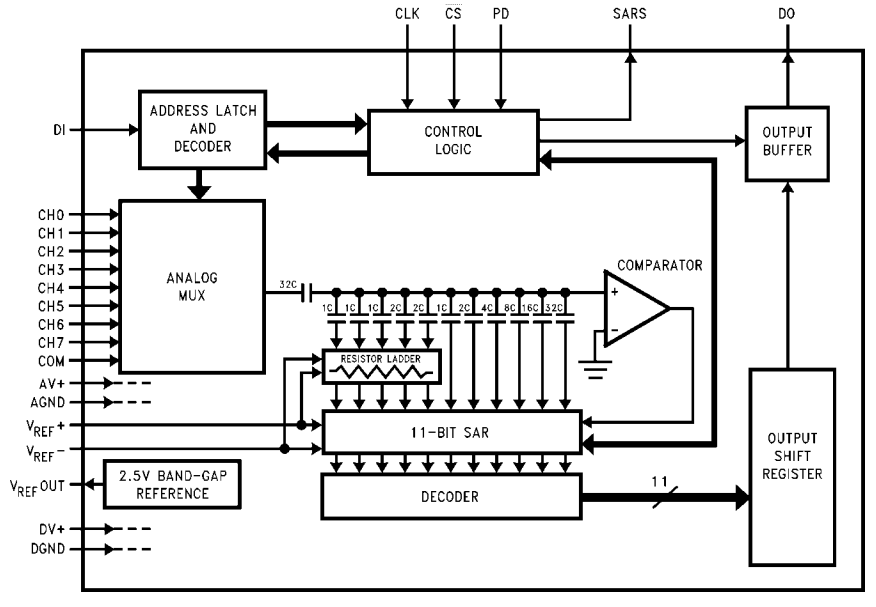
Key Specifications

Resolution	10 bits plus sign
Single supply	5V
Power consumption	37 mW (Max)
In power down mode	18 µW
Conversion time	5µs (Max)
Sampling rate	74 kHz (Max)
Band-gap reference	2.5V ±2% (Max)

Applications

- Medical instruments
- Portable and remote instrumentation
- Test equipment

ADC10738 Simplified Block Diagram



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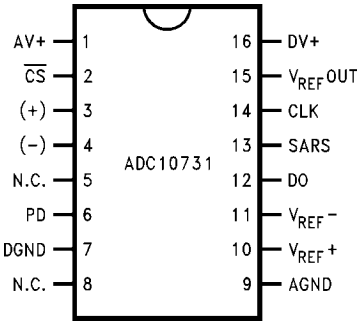
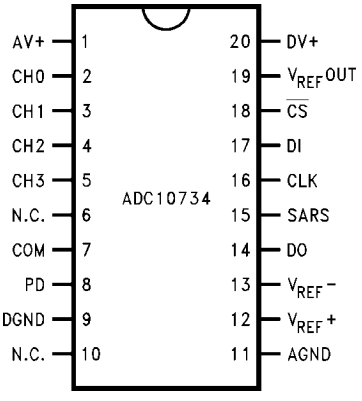
Connection Diagrams

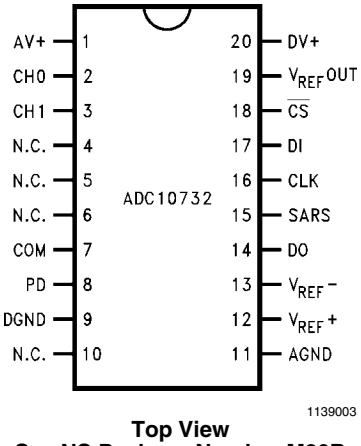
The ADC10731, ADC10732 and ADC10734 are obsolete in all packages. They are in this data sheet for reference only.



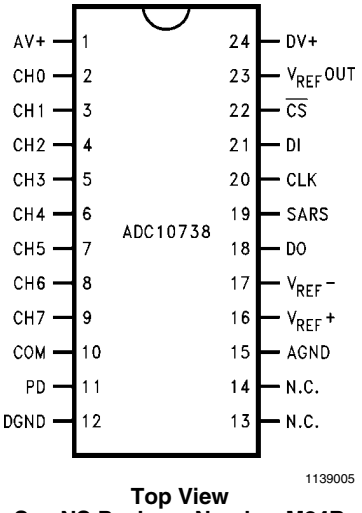
Top View
See NS Package Number M16B



Top View
See NS Package Number M20B

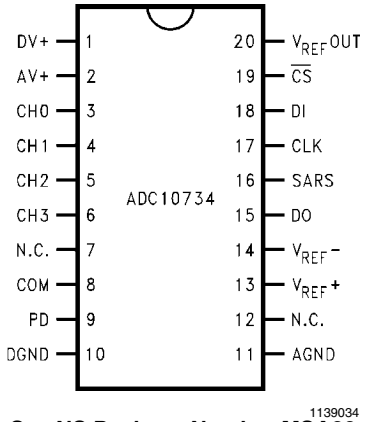


Top View
See NS Package Number M20B



Top View
See NS Package Number M24B

SSOP Package



See NS Package Number MSA20

Ordering Information

Industrial Temperature Range $-40°C \leq T_A \leq +85°C$	Package
ADC10731CIWM *	M16B
ADC10732CIWM *	M20B
ADC10734CIMSA *	MSA20
ADC10734CIWM *	M20B
ADC10738CIWM	M24B

* These products are obsolete or on lifetime buy and shown for reference only.

Pin Descriptions

CLK The clock applied to this input controls the successive approximation conversion time interval, the acquisition time and the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address shift register. This address controls which channel of the analog input multiplexer (MUX) is selected. The falling edge shifts the data resulting from the A/D conversion out on DO. $\overline{CS}$ enables or disables the above functions. The clock frequency applied to this input can be between 5 kHz and 3 MHz.

DI This is the serial data input pin. The data applied to this pin is shifted by CLK into the multiplexer address register. *Tables 1*, *2*, *3* show the multiplexer address assignment.

DO The data output pin. The A/D conversion result (DB0-SIGN) are clocked out by the failing edge of CLK on this pin.

$\overline{CS}$ This is the chip select input pin. When a logic low is applied to this pin, the rising edge of CLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE® after a conversion has been completed.

PD This is the power down input pin. When a logic high is applied to this pin the A/D is powered down. When a low is applied the A/D is powered up.

SARS This is the successive approximation register status output pin. When $\overline{CS}$ is high this pin is in TRI-STATE. With $\overline{CS}$ low this pin is active high when a conversion is in progress and active low at all other times.

CH0–CH7 These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of CLK into the address register (see *Tables 1*, *2*, *3*).

The voltage applied to these inputs should not exceed AV^+ or go below GND by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM This pin is another analog input pin. It can be used as a "pseudo ground" when the analog multiplexer is single-ended.

$V_{REF}+$ This is the positive analog voltage reference input. In order to maintain accuracy, the voltage range V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) is 0.5 V_{DC} to 5.0 V_{DC} and the voltage at $V_{REF}+$ cannot exceed AV^+ +50 mV.

$V_{REF}-$ The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND – 50 mV or exceed AV^+ + 50 mV.

AV^+, DV^+ These are the analog and digital power supply pins. These pins should be tied to the same power supply and bypassed separately. The operating voltage range of AV^+ and DV^+ is 4.5 V_{DC} to 5.5 V_{DC}.

DGND This is the digital ground pin.

AGND This is the analog ground pin.

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ = AV^+ = DV^+$)	6.5V
Total Reference Voltage ($V_{REF}+ - V_{REF}-$)	6.5V
Voltage at Inputs and Outputs	$V^+ + 0.3V$ to $-0.3V$
Input Current at Any Pin (Note 4)	30 mA
Package Input Current (Note 4)	120 mA
Package Dissipation at $T_A = 25°C$ (Note 5)	500 mW
ESD Susceptibility (Note 6)	
Human Body Model	2500V
Machine Model	150V
Soldering Information	
N packages (10 seconds)	260°C
SO Package (Note 7)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	−40°C to +150°C

Operating Ratings (Notes 3, 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
	$-40°C \le T_A \le +85°C$
Supply Voltage ($V^+ = AV^+ = DV^+$)	+4.5V to +5.5V
$V_{REF}+$	AV^+ +50 mV to −50 mV
$V_{REF}-$	AV^+ +50 mV to −50 mV
V_{REF} ($V_{REF}+ - V_{REF}-$)	+0.5V to V^+

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}+ = 2.5\ V_{DC}$, $V_{REF}- = GND$, $V_{IN}- = 2.5V$ for Signed Characteristics, $V_{IN}- = GND$ for Unsigned Characteristics and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Notes 8, 9, 10)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
SIGNED STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10 + Sign**	Bits
TUE	Total Unadjusted Error (Note 13)			**±2.0**	LSB (max)
INL	Positive and Negative Integral Linearity Error			**±1.25**	LSB (max)
	Positive and Negative Full-Scale Error			**±1.5**	LSB (max)
	Offset Error			**±1.5**	LSB (max)
	Power Supply Sensitivity				
	Offset Error	$V^+ = +5.0V \pm 10\%$	±0.2	**±1.0**	LSB (max)
	+ Full-Scale Error		±0.2	**±1.0**	LSB (max)
	− Full-Scale Error		±0.1	**±0.75**	LSB (max)
	DC Common Mode Error (Note 14)	$V_{IN}+ = V_{IN}- = V_{IN}$ where $5.0V \ge V_{IN} \ge 0V$	±0.1	**±0.33**	LSB (max)
	Multiplexer Chan to Chan Matching		±0.1		LSB
UNSIGNED STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10**	Bits
TUE	Total Unadjusted Error (Note 13)	$V_{REF}+ = 4.096V$	±0.75		LSB
INL	Integral Linearity Error	$V_{REF}+ = 4.096V$	±0.50		LSB
	Full-Scale Error	$V_{REF}+ = 4.096V$		**±1.25**	LSB (max)
	Offset Error	$V_{REF}+ = 4.096V$		**±1.25**	LSB (max)
	Power Supply Sensitivity				
	Offset Error	$V^+ = +5.0V \pm 10\%$	±0.1		LSB
	Full-Scale Error	$V_{REF}+ = 4.096V$	±0.1		LSB

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
	DC Common Mode Error (Note 14)	$V_{IN}+ = V_{IN}- = V_{IN}$ where +5.0V ≥ V_{IN} ≥ 0V	±0.1		LSB
	Multiplexer Channel to Channel Matching	$V_{REF}+ = 4.096V$	±0.1		LSB
DYNAMIC SIGNED CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	67		dB
ENOB	Effective Number of Bits	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	10.8		Bits
THD	Total Harmonic Distortion	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	−78		dB
IMD	Intermodulation Distortion	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	−85		dB
	Full-Power Bandwidth	$V_{IN} = 4.85\ V_{PP}$, where S/(N + D) Decreases 3 dB	380		kHz
	Multiplexer Chan to Chan Crosstalk	f_{IN} = 15 kHz	−80		dB
DYNAMIC UNSIGNED CONVERTER CHARACTERISTIC					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$V_{REF}+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and f_{IN} =1 kHz to 15 kHz	60		dB
ENOB	Effective Bits	$V_{REF}+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	9.8		Bits
THD	Total Harmonic Distortion	$V_{REF}+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	−70		dB
IMD	Intermodulation Distortion	$V_{REF}+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	−73		dB
	Full-Power Bandwidth	$V_{IN} = 4.0\ V_{PP}$, $V_{REF}+ = 4.096V$, where S/(N+D) decreases 3 dB	380		kHz
	Multiplexer Chan to Chan Crosstalk	f_{IN} = 15 kHz, $V_{REF}+ = 4.096V$	−80		dB
REFERENCE INPUT AND MULTIPLEXER CHARACTERISTICS					
	Reference Input Resistance		7	**5.0** **9.5**	kΩ kΩ(min) kΩ(max)
C_{REF}	Reference Input Capacitance		70		pF
	MUX Input Voltage			**−50** **AV^+ + 50mV**	mV (min) (max)
C_{IM}	MUX Input Capacitance		47		pF
	Off Channel Leakage Current (Note 15)	On Channel = 5V and Off Channel = 0V	−0.4	**−3.0**	µA (max)
		On Channel = 0V and Off Channel = 5V	0.4	**3.0**	µA (max)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
	On Channel Leakage Current (Note 15)	On Channel = 5V and Off Channel = 0V	0.4	**3.0**	µA (max)
		On Channel = 0V and Off Channel = 5V	−0.4	**−3.0**	µA (max)
REFERENCE CHARACTERISTICS					
V_{REF}Out	Reference Output Voltage		2.5V ±0.5%	**2.5V ±2%**	V (max)
$\Delta V_{REF}/\Delta T$	V_{REF}Out Temperature Coefficient		±40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation, Sourcing	0 mA ≤ I_L ≤ +4 mA	±0.003	**±0.05**	%/mA (max)
$\Delta V_{REF}/\Delta I_L$	Load Regulation, Sinking	0 mA ≤ I_L ≤ −1 mA	±0.2	**±0.6**	%/mA (max)
	Line Regulation	5V ±10%	±0.3	**±2.5**	mV (max)
I_{SC}	Short Circuit Current	V_{REF}Out = 0V	13	**22**	mA (max)
	Noise Voltage	10 Hz to 10 kHz, C_L = 100 µF	5		µV
$\Delta V_{REF}/\Delta t$	Long-term Stability		±120		ppm/kHr
t_{SU}	Start-Up Time	C_L = 100 µF	100		ms
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage	V^+ = 5.5V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V^+ = 4.5V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 5.0V	0.005	**+2.5**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	−0.005	**−2.5**	µA (max)
$V_{OUT(1)}$	Logical “1” Output Voltage	V^+ = 4.5V, I_{OUT} = −360 µA		**2.4**	V (min)
		V^+ = 4.5V, I_{OUT} = −10 µA		**4.5**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V^+ = 4.5V, I_{OUT} = 1.6 mA		**0.4**	V (min)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 0V	−0.1	**−3.0**	µA (max)
		V_{OUT} = 5V	+0.1	**+3.0**	µA (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V, V^+ = 4.5V	−30	**−15**	mA(min)
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT}= V^+ = 4.5V	30	**15**	mA (min)
I_D+	Digital Supply Current (Note 17)	$\overline{CS}$ = HIGH, Power Up	0.9	**1.3**	mA (max)
		$\overline{CS}$ = HIGH, Power Down	0.2	**0.4**	mA (max)
		$\overline{CS}$ = HIGH, Power Down, and CLK Off	0.5	**50**	µA (max)
I_A+	Analog Supply Current (Note 17)	$\overline{CS}$ = HIGH, Power Up	2.7	**6.0**	mA (max)
		$\overline{CS}$ = HIGH, Power Down	3	**15**	µA (max)
I_{REF}	Reference Input Current	V_{REF}+ = +2.5V and $\overline{CS}$ = HIGH, Power Up		**0.6**	mA (max)
AC CHARACTERISTICS					
f_{CLK}	Clock Frequency		3.0	**2.5**	MHz (max)
			5		kHz (min)
	Clock Duty Cycle			**40**	%(min)
				60	%(max)
t_C	Conversion Time		12	**12**	Clock Cycles
			5	**5**	µs (max)
t_A	Acquisition Time		4.5	**4.5**	Clock Cycles
			2	**2**	µs (max)
t_{SCS}	$\overline{CS}$ Set-Up Time, Set-Up Time from Falling Edge of CS to Rising Edge of Clock		14 (1 t_{CLK} − 14 ns)	**30 (1 t_{CLK} − 30 ns)**	ns (min) (max)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
t_{SDI}	DI Set-Up Time, Set-Up Time from Data Valid on DI to Rising Edge of Clock		16	**25**	ns (min)
t_{HDI}	DI Hold Time, Hold Time of DI Data from Rising Edge of Clock to Data not Valid on DI		2	**25**	ns (min)
t_{AT}	DO Access Time from Rising Edge of CLK When $\overline{CS}$ is "Low" during a Conversion		30	**50**	ns (min)
t_{AC}	DO or SARS Access Time from $\overline{CS}$, Delay from Falling Edge of $\overline{CS}$ to Data Valid on DO or SARS		30	**70**	ns (max)
t_{DSARS}	Delay from Rising Edge of Clock to Falling Edge of SARS when $\overline{CS}$ is "Low"		100	**200**	ns (max)
t_{HDO}	DO Hold Time, Hold Time of Data on DO after Falling Edge of Clock		20	**35**	ns (max)
t_{AD}	DO Access Time from Clock, Delay from Falling Edge of Clock to Valid Data of DO		40	**80**	ns (max)
t_{1H}, t_{0H}	Delay from Rising Edge of $\overline{CS}$ to DO or SARS TRI-STATE		40	**50**	ns (max)
t_{DCS}	Delay from Falling Edge of Clock to Falling Edge of $\overline{CS}$		20	**30**	ns (min)
$t_{CS(H)}$	$\overline{CS}$ "HIGH" Time for A/D Reset after Reading of Conversion Result		1 CLK	**1 CLK**	cycle (min)
$t_{CS(L)}$	ADC10731 Minimum $\overline{CS}$ "Low" Time to Start a Conversion		1 CLK	**1 CLK**	cycle (min)
t_{SC}	Time from End of Conversion to $\overline{CS}$ Going "Low"		5 CLK	**5 CLK**	cycle (min)
t_{PD}	Delay from Power-Down command to 10% of Operating Current		1		µs
t_{PC}	Delay from Power-Up Command to Ready to Start a New Conversion		10		µs
C_{IN}	Capacitance of Logic Inputs		7		pF
C_{OUT}	Capacitance of Logic Outputs		12		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > AV+ or DV+), the current at that pin should be limited to 30 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given In the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 150°C. The typical thermal resistance (θ_{JA}) of these Paris when board mounted can be found in the following table:

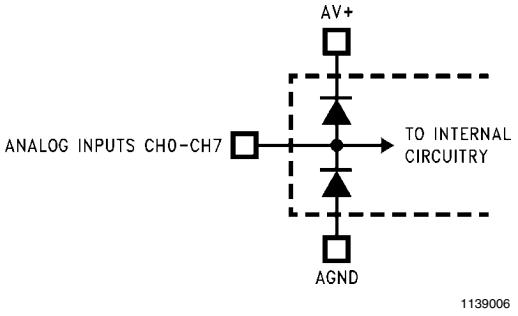
Part Number	Thermal Resistance	Package Type
ADC10731CIWM	90°C/W	M16B
ADC10732CIWM	80°C/W	M20B
ADC10734CIMSA	134°C/W	MSA20
ADC10734CIWM	80°C/W	M20B
ADC10738CIWM	75°C/W	M24B

Note 6: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 7: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 8: Two on-chip diodes are tied to each analog input as shown below. They will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V+ supply. Be careful during testing at low V+ levels (+4.5V), as high level analog inputs (+5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors In the conversion result. The specification allows 50 mV forward bias of either diode; this means that

as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. If AV+ and DV+ are minimum (4.5 V_{DC}) and full scale must be ≤+4.55 V_{DC}.



Note 9: No connection exists between AV+ and DV+ on the chip.

To guarantee accuracy, it is required that the AV+ and DV+ be connected together to a power supply with separate bypass filter at each V+ pin.

Note 10: One LSB is referenced to 10 bits of resolution.

Note 11: Typicals are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

Note 12: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 13: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 14: The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.

Note 15: Channel leakage current is measured after the channel selection.

Note 16: All the timing specifications are tested at the TTL logic levels, V_{IL} = 0.8V for a falling edge and V_{IH} = 2.0V for a rising. TRI-STATE voltage level is forced to 1.4V.

Note 17: The voltage applied to the digital inputs will affect the current drain during power down. These devices are tested with CMOS logic levels (logic Low = 0V and logic High = 5V). TTL levels increase the current, during power down, to about 300 µA.

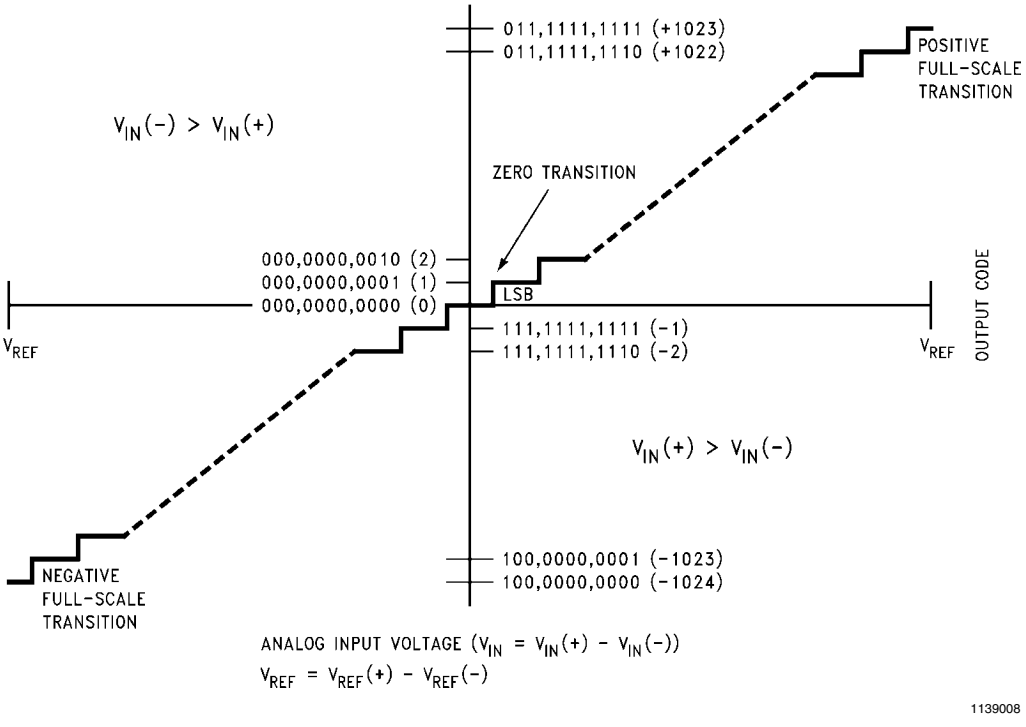


FIGURE 1. Transfer Characteristic

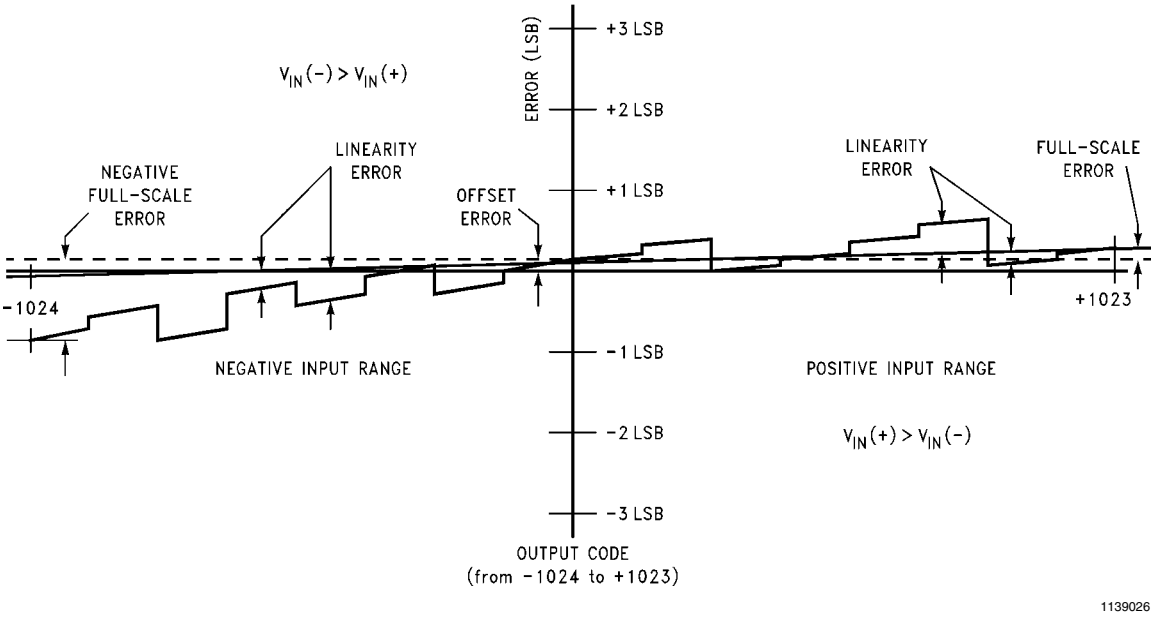
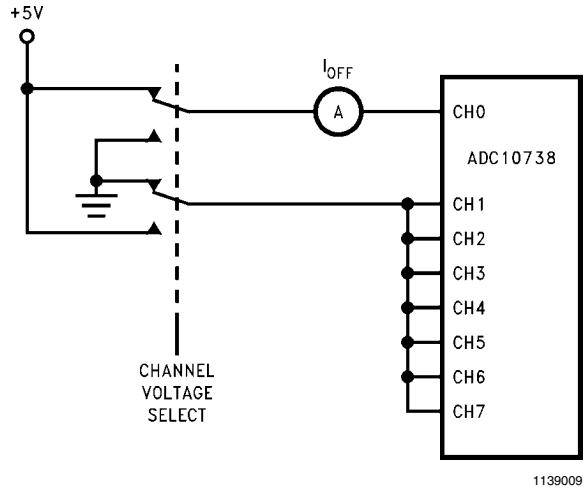


FIGURE 2. Simplified Error Curve vs. Output Code

Test Circuit

Leakage Current Test Circuit



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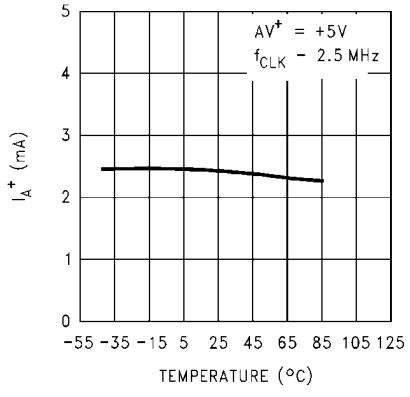
Typical Performance Characteristics

Analog Supply Current (I_A+) vs. Temperature



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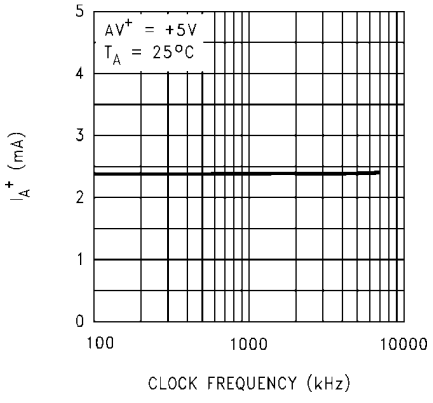
Analog Supply Current (I_A+) vs. Clock Frequency



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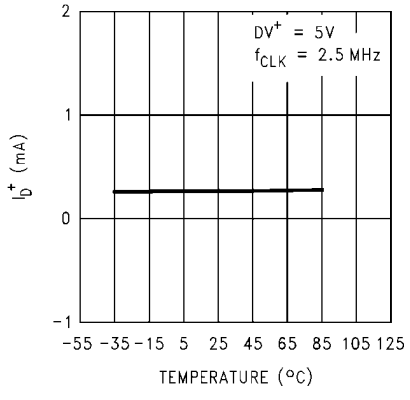
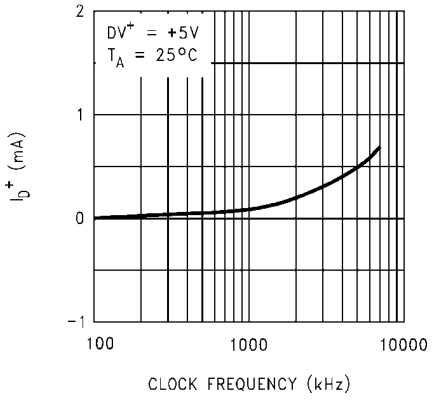
Digital Supply Current (I_D+) vs. Temperature



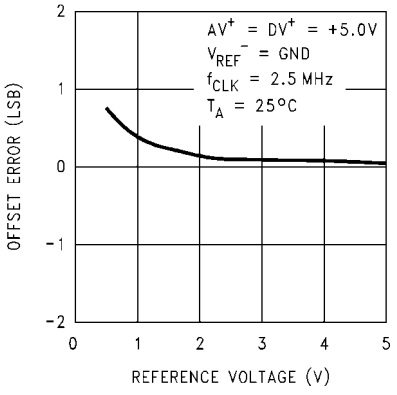
1139037

Digital Supply Current (I_D+) vs. Clock Frequency



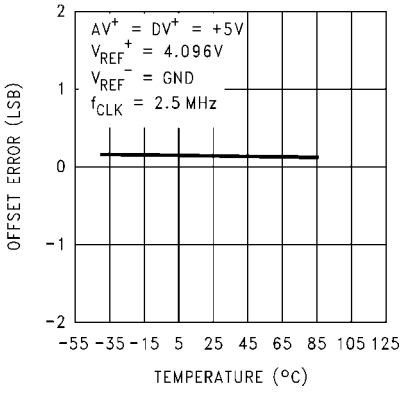
1139038

Offset Error vs. Reference Voltage



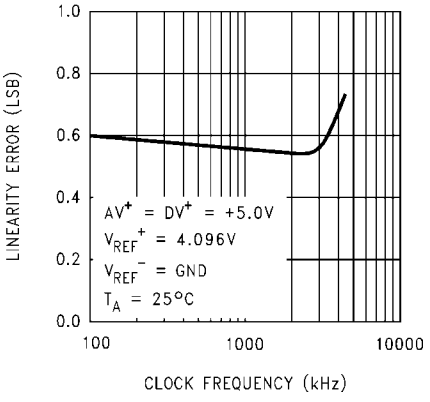
1139039

Offset Error vs. Temperature



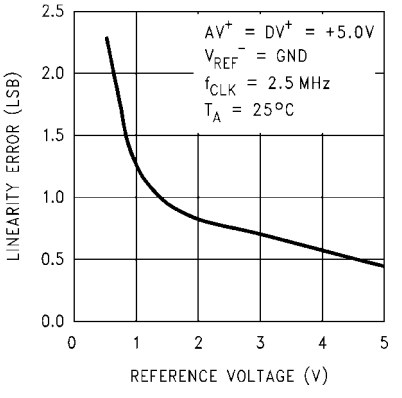
1139040

Linearity Error vs. Clock Frequency



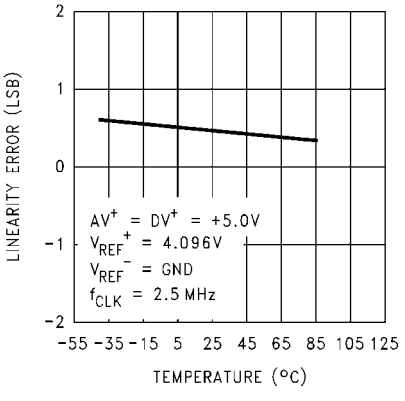
1139041

Linearity Error vs. Reference Voltage



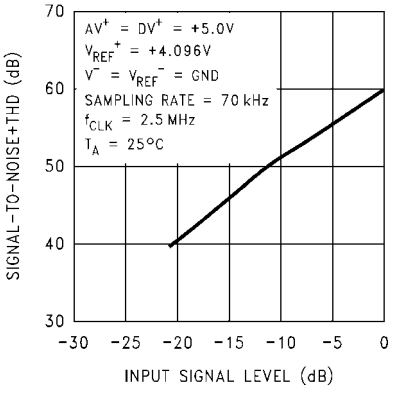
1139042

Linearity Error vs. Temperature



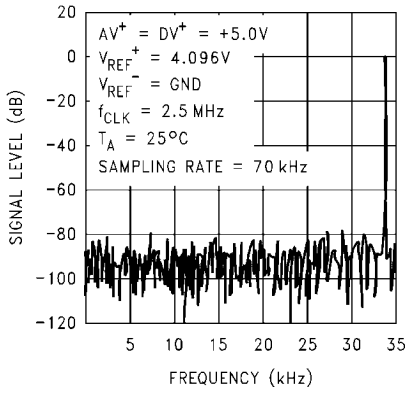
1139043

10-Bit Unsigned Signal-to-Noise + THD Ratio vs. Input Signal Level



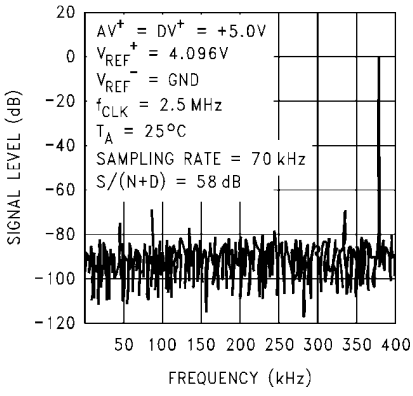
1139044

Spectral Response with 34 kHz Sine Wave



1139045

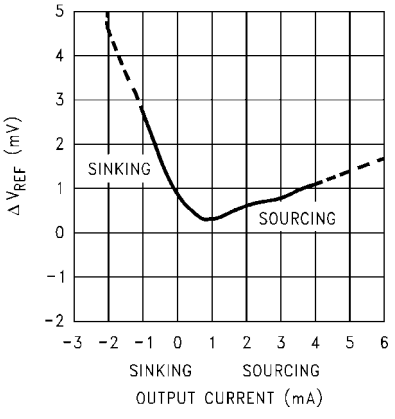
Power Bandwidth Response with 380 kHz Sine Wave



1139046

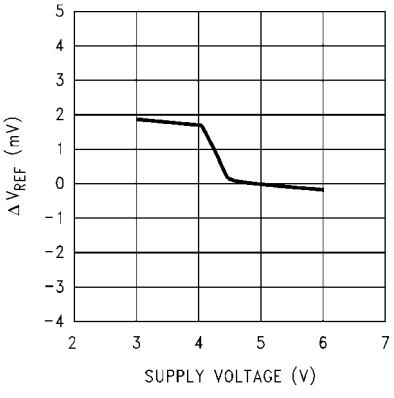
Typical Reference Performance Characteristics

Load Regulation



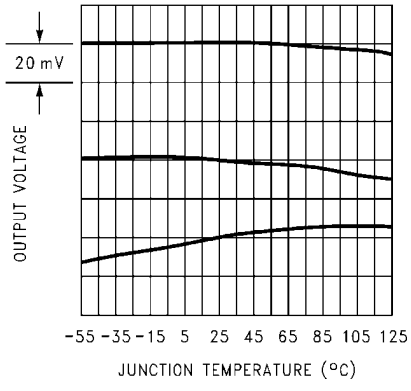
1139047

Line Regulation



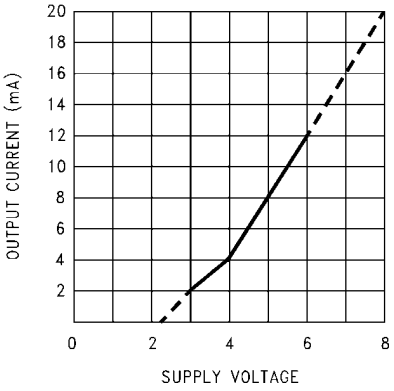
1139048

Output Drift vs. Temperature (3 Typical Parts)



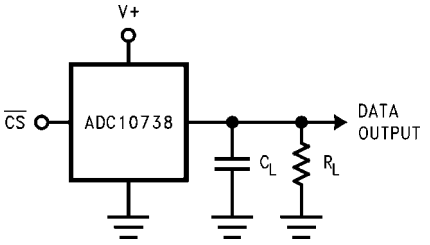
1139049

Available Output Current vs. Supply Voltage

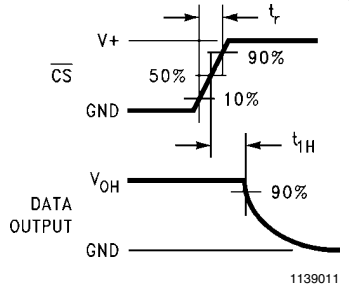


1139050

TRI-STATE Test Circuits and Waveforms



1139010



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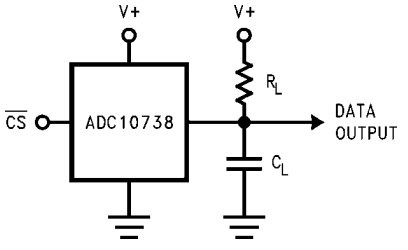
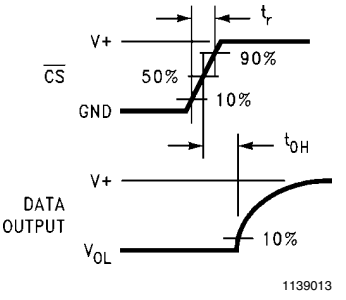
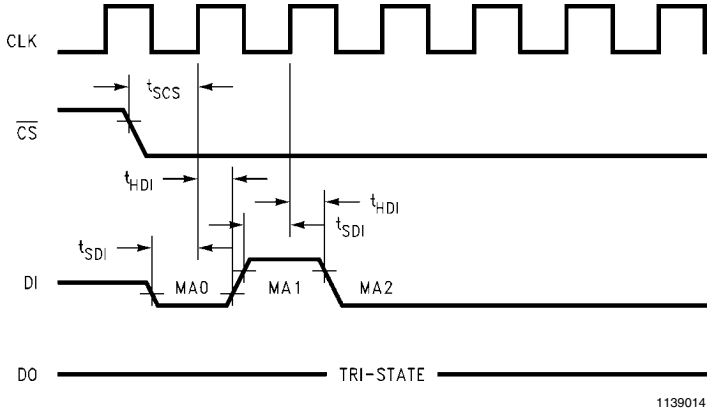


1139012



1139013

Timing Diagrams



1139014

FIGURE 3. DI Timing

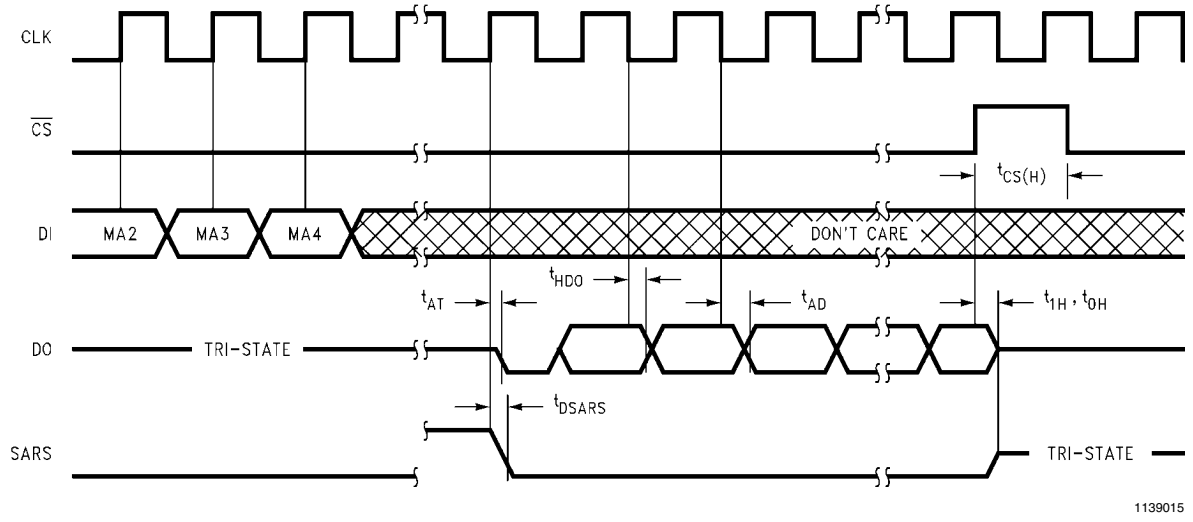


FIGURE 4. DO Timing

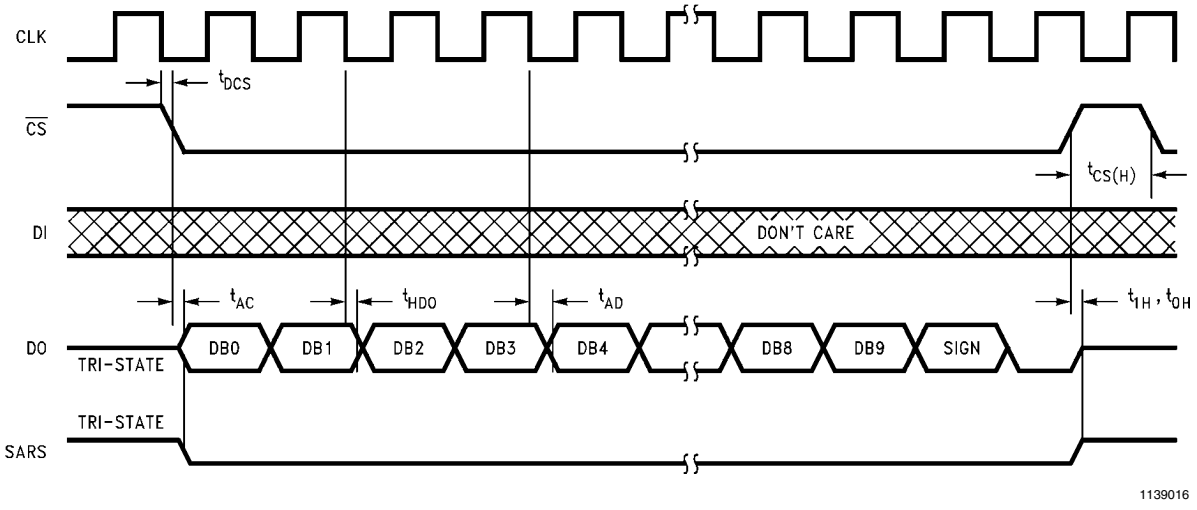


FIGURE 5. Delayed DO Timing

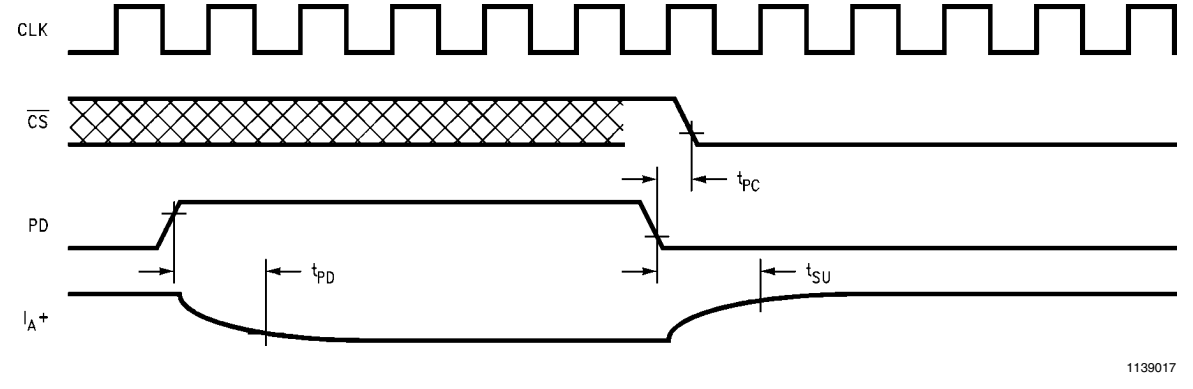


FIGURE 6. Hardware Power Up/Down Sequence

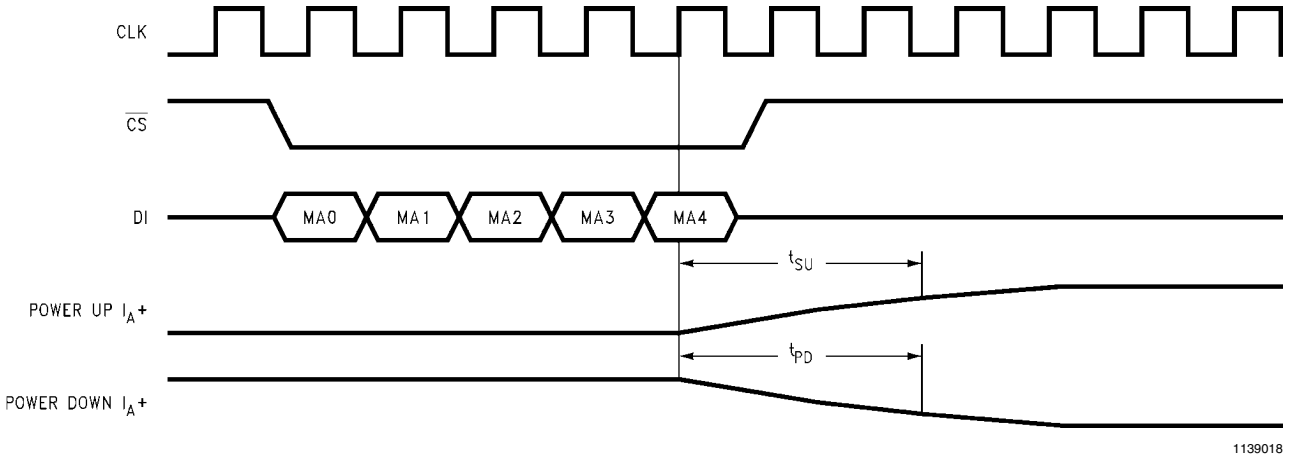
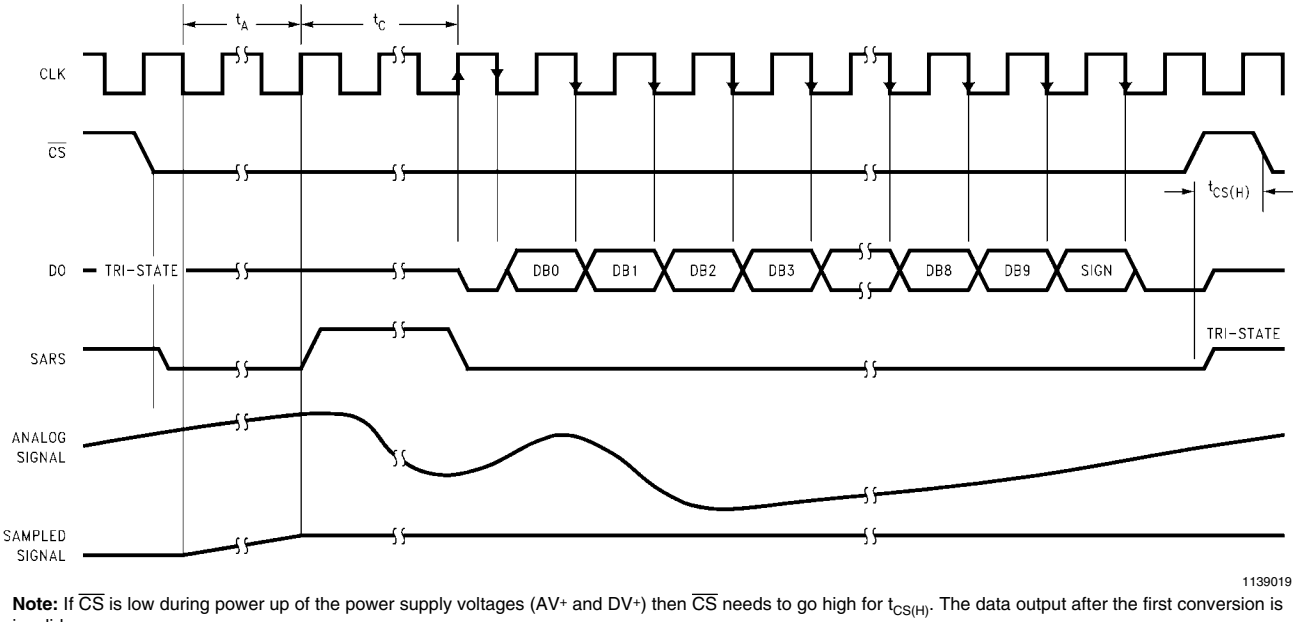


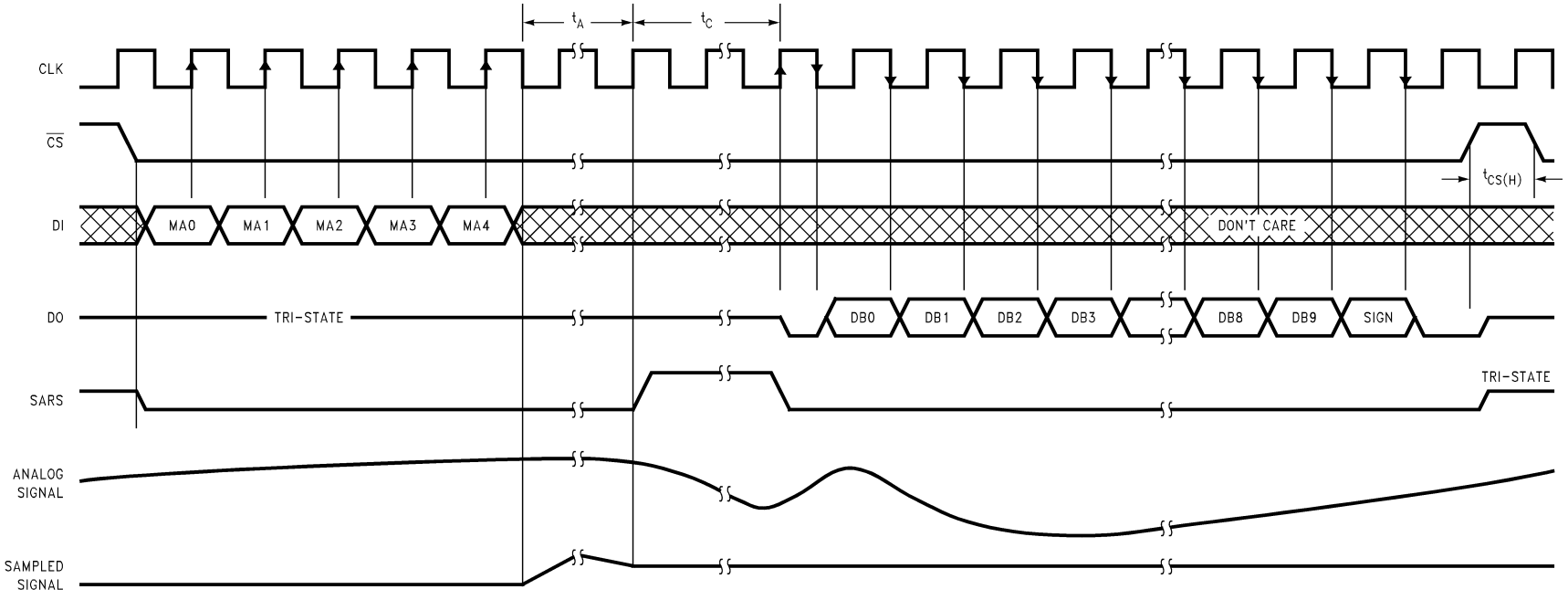
FIGURE 7. Software Power Up/Down Sequence



Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is invalid.

The ADC10731 is obsolete. Information shown for reference only.

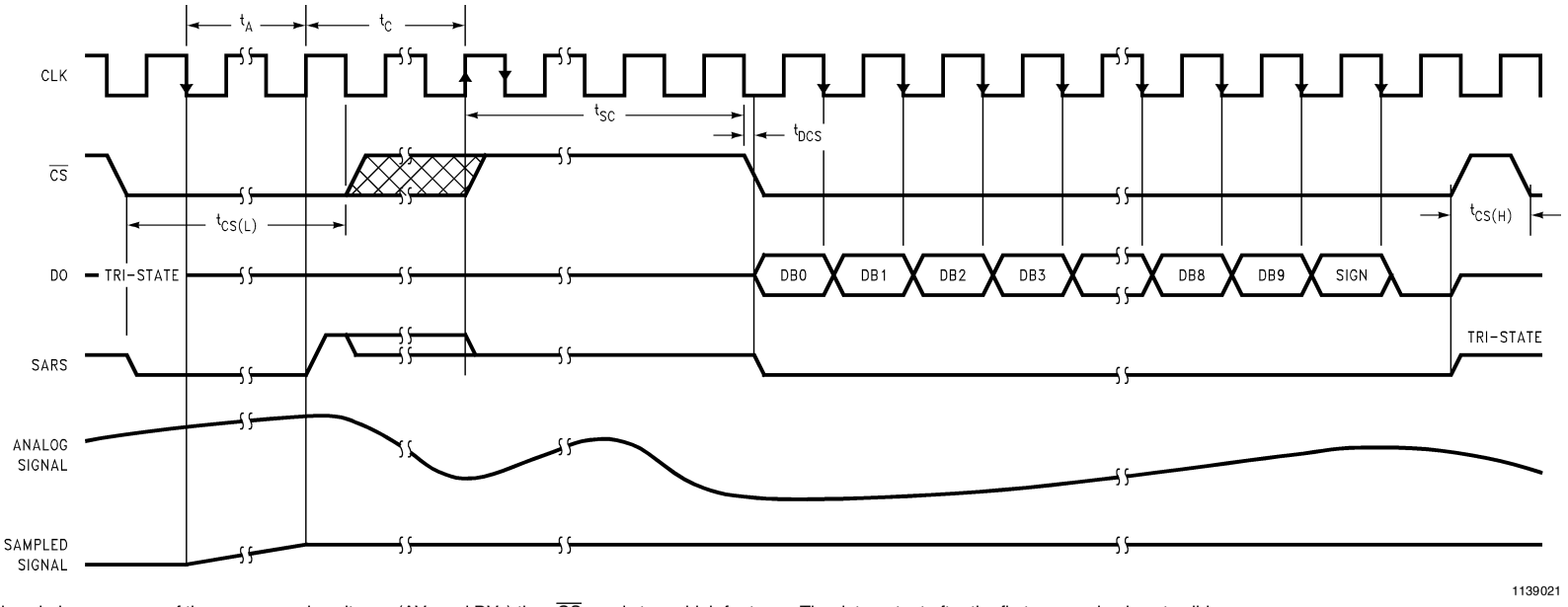
FIGURE 8. ADC10731 $\overline{CS}$ Low during Conversion



Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

The ADC10732 and the ADC10734 are obsolete. Information shown for reference only.

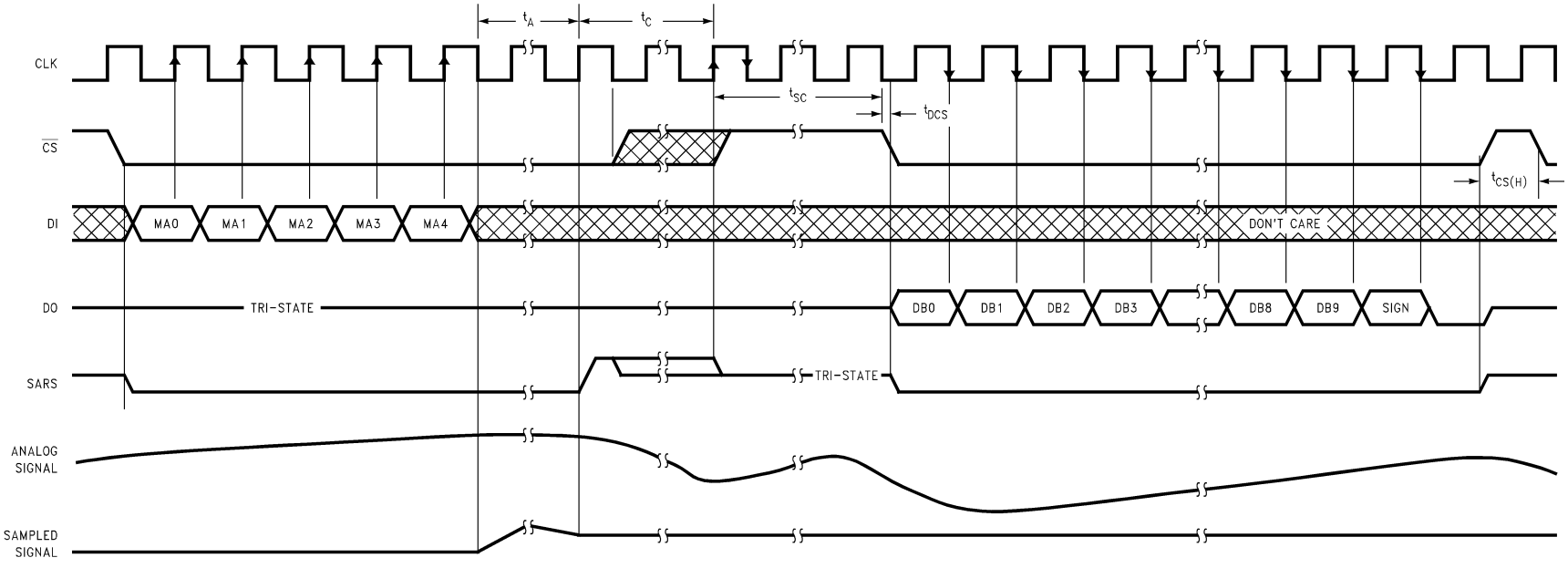
FIGURE 9. ADC10732, ADC10734 and ADC10738 $\overline{CS}$ Low during Conversion



Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

The ADC10731 is obsolete. Information shown for reference only.

FIGURE 10. ADC10731 Using $\overline{CS}$ to Delay Output of Data after a Conversion has Completed



Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

The ADC10732 and the ADC10734 are obsolete. Information shown for reference only.

FIGURE 11. ADC10732, ADC10734 and ADC10738 Using $\overline{CS}$ to Delay Output of Data after a Conversion has Completed

TABLE 1. ADC10738 Multiplexer Address Assignment

MUX Address					Channel Number									MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0										
1	1	0	0	0	+								−	
1	1	0	0	1			+						−	
1	1	0	1	0					+				−	
1	1	0	1	1							+		−	Single-Ended
1	1	1	0	0		+							−	
1	1	1	0	1				+					−	
1	1	1	1	0						+			−	
1	1	1	1	1								+	−	
1	0	0	0	0	+	−								
1	0	0	0	1			+	−						
1	0	0	1	0					+	−				
1	0	0	1	1							+	−		Differential
1	0	1	0	0	−	+								
1	0	1	0	1			−	+						
1	0	1	1	0					−	+				
1	0	1	1	1							−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)									

TABLE 2. ADC10734 (Obsolete) Multiplexer Address Assignment

MUX Address					Channel Number					MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	CH2	CH3	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0						
1	1	0	0	0	+				−	
1	1	0	0	1			+		−	Single-Ended
1	1	1	0	0		+			−	
1	1	1	0	1				+	−	
1	0	0	0	0	+	−				
1	0	0	0	1			+	−		Differential
1	0	1	0	0	−	+				
1	0	1	0	1			−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)					

TABLE 3. ADC10732 (Obsolete) Multiplexer Address Assignment

MUX Address					Channel Number			MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	COM	
PU	SING/DIFF	ODD/SIGN	SEL1	SEL0				
1	1	0	0	0	+		−	Single-Ended
1	1	1	0	0		+	−	
1	0	0	0	0	+	−		Differential
1	0	1	0	0	−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)			

Applications Hints

The ADC10731, ADC10732 and ADC10734 are obsolete and discussed here for reference only.

The ADC10731/2/4/8 use successive approximation to digitize an analog input voltage. The DAC portion of the A/D converters uses a capacitive array and a resistive ladder structure. The structure of the DAC allows a very simple switching scheme to provide a versatile analog input multiplexer. This structure also provides a sample/hold. The ADC10731/2/4/8 have a 2.5V CMOS bandgap reference. The serial digital I/O interfaces to MICROWIRE and MICROWIRE+.

1.0 DIGITAL INTERFACE

There are two modes of operation. The fastest throughput rate is obtained when $\overline{CS}$ is kept low during a conversion. The timing diagrams in *Figures 8*, *9* show the operation of the devices in this mode. $\overline{CS}$ must be taken high for at least $t_{CS(H)}$ (1 CLK) between conversions. This is necessary to reset the internal logic. *Figures 10*, *11* show the operation of the devices when $\overline{CS}$ is taken high while the ADC10731/2/4/8 is converting. $\overline{CS}$ may be taken high during the conversion and kept high indefinitely to delay the output data. This mode simplifies the interface to other devices while the ADC10731/2/4/8 is busy converting.

1.1 Getting Started with a Conversion

The ADC10731/2/4/8 need to be initialized after the power supply voltage is applied. If $\overline{CS}$ is low when the supply voltage is applied then $\overline{CS}$ needs to be taken high for at least $t_{CS(H)}$(1 clock period). The data output after the first conversion is not valid.

1.2 Software and Hardware Power Up/Down

These devices have the capability of software or hardware power down. *Figures 6*, *7* show the timing diagrams for hardware and software power up/down. In the case of hardware power down note that $\overline{CS}$ needs to be high for t_{PC} after PD is taken low. When PD is high the device is powered down. The total quiescent current, when powered down, is typically 200 µA with the clock at 2.5 MHz and 3 µA with the clock off. The actual voltage level applied to a digital input will effect the power consumption of the device during power down. CMOS logic levels will give the least amount of current drain (3 µA). TTL logic levels will increase the total current drain to 200 µA.

These devices have resistive reference ladders which draw 600 µA with a 2.5V reference voltage. The internal band gap reference voltage shuts down when power down is activated. If an external reference voltage is used, it will have to be shut down to minimize the total current drain of the device.

2.0 ARCHITECTURE

Before a conversion is started, during the analog input sampling period, (t_A), the sampled data comparator is zeroed. As the comparator is being zeroed the channel assigned to be the positive input is connected to the A/D's input capacitor. (The assignment procedure is explained in the Pin Descriptions section.) This charges the input 32C capacitor of the DAC to the positive analog input voltage. The switches shown in the DAC portion of *Figure 12* are set for this zeroing/acquisition period. The voltage at the input and output of the comparator are at equilibrium at this time. When the conversion is started, the comparator feedback switches are opened and the 32C input capacitor is then switched to the assigned negative input voltage. When the comparator feedback switch opens, a fixed amount of charge is trapped on the common plates of the capacitors. The voltage at the input of the comparator moves away from equilibrium when the 32C capacitor is switched to the assigned negative input voltage, causing the output of the comparator to go high (“1”) or low (“0”). The SAR next goes through an algorithm, controlled by the output state of the comparator, that redistributes the charge on the capacitor array by switching the voltage on one side of the capacitors in the array. The objective of the SAR algorithm is to return the voltage at the input of the comparator as close as possible to equilibrium.

The switch position information at the completion of the successive approximation routine is a direct representation of the digital output. This data is then available to be shifted on the DO pin.

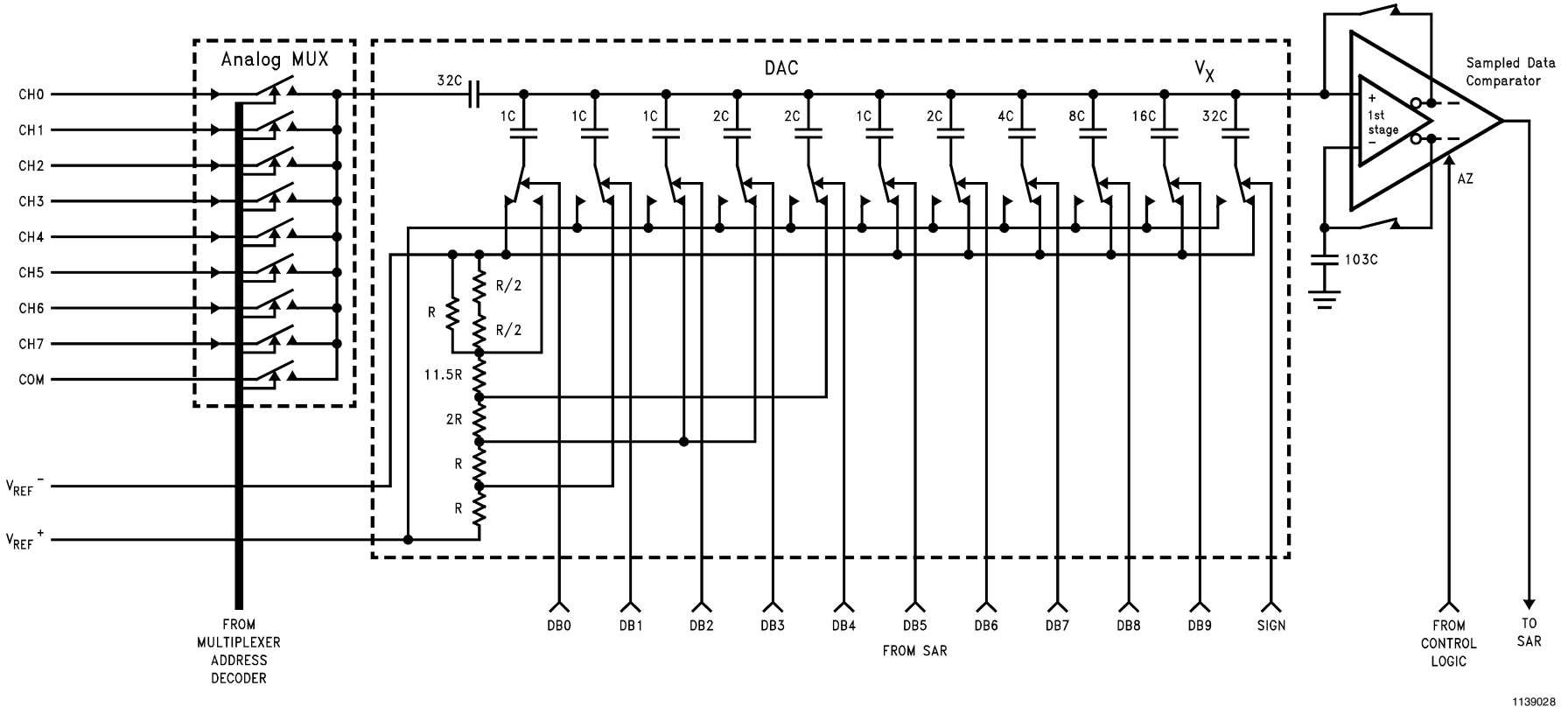


FIGURE 12. Detailed Diagram of the ADC10738 DAC and Analog Multiplexer Stages

3.0 APPLICATIONS INFORMATION

3.1 Multiplexer Configuration

The design of these converters utilizes a sampled-data comparator structure, which allows a differential analog input to be converted by the successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "–" input terminal. The polarity of each input terminal or pair of input terminals being converted indicates which line the converter expects to be the most positive.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-ended, or pseudo-differential. *Figure 13* illustrates the three modes using the 4-channel MUX of the ADC10734. The eight inputs of the ADC10738 can also be configured in any of the three modes. The single-ended mode has CH0–CH3 assigned as the positive input with COM serving as the negative input. In the differential mode, the ADC10734 channel inputs are grouped in pairs, CH0 with CH1 and CH2 with CH3. The polarity assignment of each channel in the pair is interchangeable. Finally, in the pseudo-differential mode CH0–CH3 are positive inputs referred to COM which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground-referred inputs and true differential inputs as well as signals referred to a specific voltage.

The analog input voltages for each channel can range from 50 mV below GND to 50 mV above $V^+ = DV^+ = AV^+$ without degrading conversion accuracy. If the voltage on an unselected channel exceeds these limits it may corrupt the reading of the selected channel.

3.2 Reference Considerations

The voltage difference between the V_{REF}^+ and V_{REF}^- inputs defines the analog input voltage span (the difference between V_{IN}(Max) and V_{IN}(Min)) over which 1023 positive and 1024 negative possible output codes apply.

The value of the voltage on the V_{REF}^+ or V_{REF}^- inputs can be anywhere between AV^+ + 50 mV and –50 mV, so long as V_{REF}^+ is greater than V_{REF}^-. The ADC10731/2/4/8 can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the minimum reference input resistance of 5 kΩ.

The internal 2.5V bandgap reference in the ADC10731/2/4/8 is available as an output on the VREFOut pin. To ensure optimum performance this output needs to be bypassed to ground with 100 µF aluminum electrolytic or tantalum capacitor. The reference output can be unstable with capacitive loads greater than 100 pF and less than 100 µF. Any capacitive loading less than 100 pF and greater than 100 µF will not cause oscillation. Lower output noise can be obtained by increasing the output capacitance. A 100 µF capacitor will yield a typical noise floor of

$$200\ nV/\sqrt{Hz}$$

.

The pseudo-differential and differential multiplexer modes allow for more flexibility in the analog input voltage range since the "zero" reference voltage is set by the actual voltage applied to the assigned negative input pin.

In a ratiometric system (*Figure 14*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage may also be the system power supply, so V_{REF}+ can also be tied to AV^+. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 15*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time- and temperature-stable voltage source that has excellent initial accuracy. The LM4040, LM4041 and LM185 references are suitable for use with the ADC10731/2/4/8.

The minimum value of V_{REF} ($V_{REF} = V_{REF}+–V_{REF}–$) can be quite small (see Typical Performance Characteristics) to allow direct conversion of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/1024).

3.3 The Analog Inputs

Due to the sampling nature of the analog inputs, at the clock edges short duration spikes of current will be seen on the selected assigned negative input. Input bypass capacitors should not be used if the source resistance is greater than 1 kΩ since they will average the AC current and cause an effective DC current to flow through the analog input source resistance. An op amp RC active lowpass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required. Bypass capacitors may be used when the source impedance is very low without any degradation in performance.

In a true differential input stage, a signal that is common to both "+" and "–" inputs is canceled. For the ADC10731/2/4/8, the positive input of a selected channel pair is only sampled once before the start of a conversion during the acquisition time (t_A). The negative input needs to be stable during the complete conversion sequence because it is sampled before each decision in the SAR sequence. Therefore, any AC common-mode signal present on the analog inputs will not be completely canceled and will cause some conversion errors. For a sinusoid common-mode signal this error is:

$V_{ERROR}(max) = V_{PEAK}\ (2\ \pi\ f_{CM})\ (t_C)$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value, and t_C is the A/D's conversion time ($t_C = 12/f_{CLK}$). For example, for a 60 Hz common-mode signal to generate a ¼ LSB error (0.61 mV) with a 4.8 µs conversion time, its peak value would have to be approximately 337 mV.

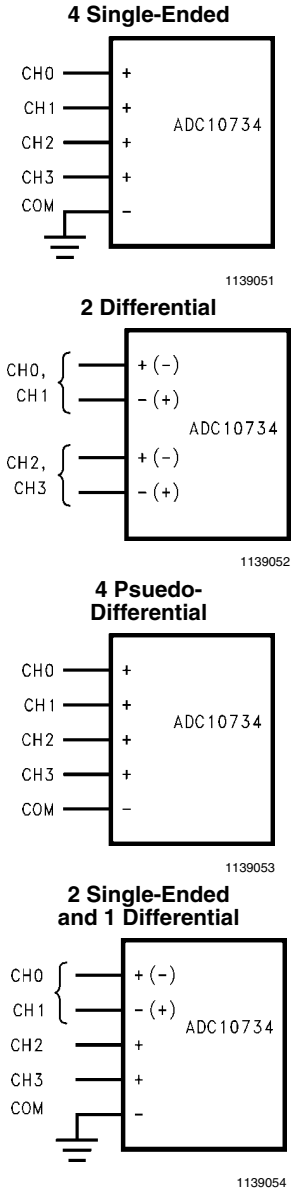


FIGURE 13. Analog Input Multiplexer Options

Ratiometric Using the Internal Reference

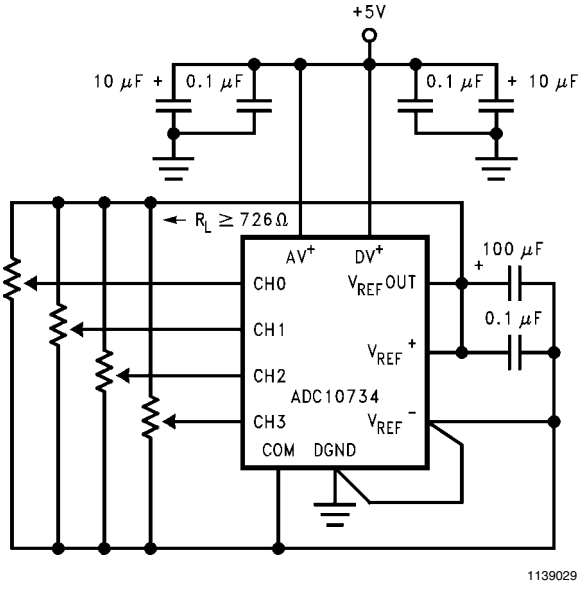


FIGURE 14.

Absolute Using a 4.096V Span

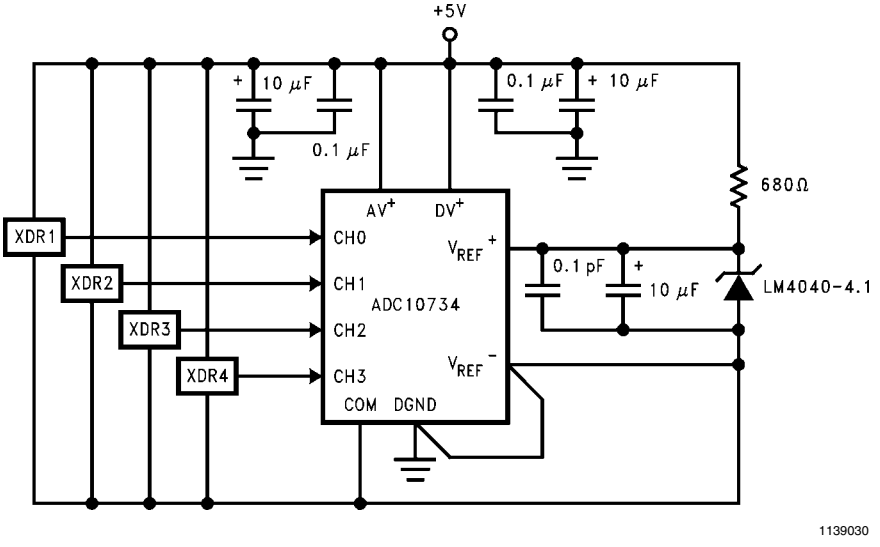


FIGURE 15. Different Reference Configurations

3.4 Optional Adjustments

3.4.1 Zero Error

The zero error of the A/D converter relates to the location of the first riser of the transfer function (see *Figures 1*, *2*) and can be measured by grounding the minus input and applying a small magnitude voltage to the plus input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 000 0000 0000 to 000 0000 0001 and the ideal ½ LSB value (½ LSB = 1.22 mV for V_{REF} = + 2.500V).

The zero error of the A/D does not require adjustment. If the minimum analog input voltage value, V_{IN}(Min), is not ground, the effective "zero" voltage can be adjusted to a convenient value. The converter can be made to output an all zeros digital code for this minimum input voltage by biasing any minus input to V_{IN}(Min). This is useful for either the differential or pseudo-differential input channel configurations.

3.4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the V_{REF} voltage ($V_{REF} = V_{REF}^{+} - V_{REF}^{-}$) for a digital output code changing from 011 1111 1110 to 011 1111 1111. In bipolar signed operation this only adjusts the positive full scale error.

3.4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A plus input voltage which equals this desired zero reference plus ½ LSB is applied to selected plus input and the zero reference voltage at the corresponding minus input should then be adjusted to just obtain the 000 0000 0000 to 000 0000 0001 code transition.

The full-scale adjustment should be made [with the proper minus input voltage applied] by forcing a voltage to the plus input which is given by:

$$V_{IN}(+)\, f_s\, adj = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{2^n} \right]$$

where V_{MAX} equals the high end of the analog input range, V_{MIN} equals the low end (the offset zero) of the analog range. Both V_{MAX} and V_{MIN} are ground referred. The V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) voltage is then adjusted to provide a code change from 011 1111 1110 to 011 1111 1111. Note, when using a pseudo-differential or differential multiplexer mode where V_{REF}+ and V_{REF}– are placed within the V+ and GND range, the individual values of V_{REF} and V_{REF}– do not matter, only the difference sets the analog input voltage span. This completes the adjustment procedure.

3.5 The Input Sample and Hold

The ADC10731/2/4/8's sample/hold capacitor is implemented in the capacitor array. After the channel address is loaded, the array is switched to sample the selected positive analog input. The sampling period for the assigned positive input is maintained for the duration of the acquisition time (t_A) 4.5 clock cycles.

This acquisition window of 4.5 clock cycles is available to allow the voltage on the capacitor array to settle to the positive analog input voltage. Any change in the analog voltage on a selected positive input before or after the acquisition window will not effect the A/D conversion result.

In the simplest case, the array's acquisition time is determined by the R_{ON} (3 kΩ) of the multiplexer switches, the stray input capacitance C_{S1} (3.5 pF) and the total array (C_L) and stray (C_{S2}) capacitance (48 pF). For a large source resistance the analog input can be modeled as an RC network as shown in *Figure 16*. The values shown yield an acquisition time of about 1.1 µs for 10-bit unipolar or 10-bit plus sign accuracy with a zero-to-full-scale change in the input voltage. External source resistance and capacitance will lengthen the acquisition time and should be accounted for. Slowing the clock will lengthen the acquisition time, thereby allowing a larger external source resistance.

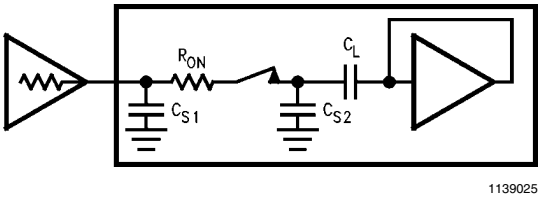
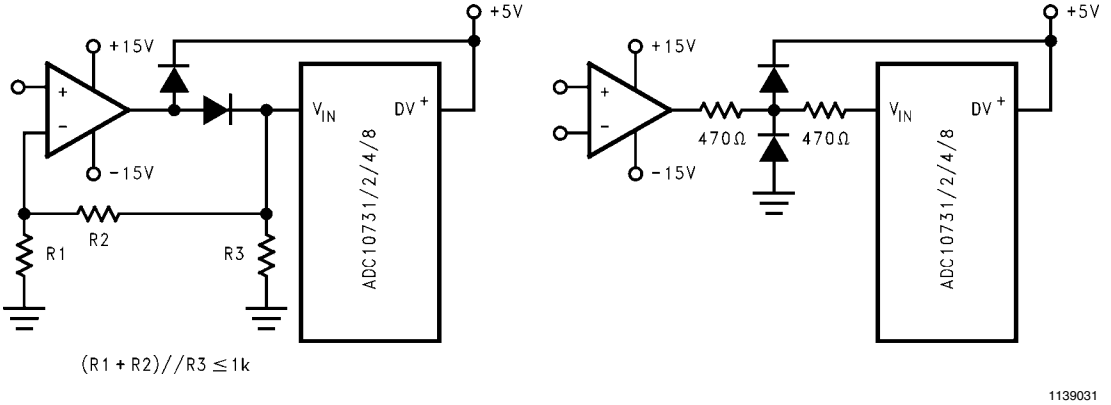


FIGURE 16. Analog Input Model

The signal-to-noise ratio of an ideal A/D is the ratio of the RMS value of the full scale input signal amplitude to the value of the total error amplitude (including noise) caused by the transfer function of the ideal A/D. An ideal 10-bit plus sign A/D converter with a total unadjusted error of 0 LSB would have a signal-to-(noise + distortion) ratio of about 68 dB, which can be derived from the equation:

S/(N + D) = 6.02(n) + 1.76

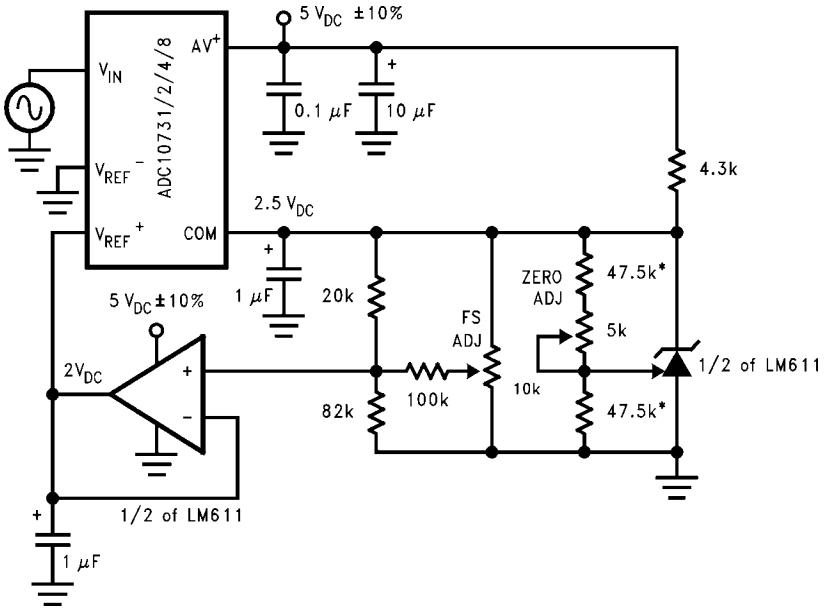
where S/(N + D) is in dB and n is the number of bits.



Note: Diodes are 1N914.

Note: The protection diodes should be able to withstand the output current of the op amp under current limit.

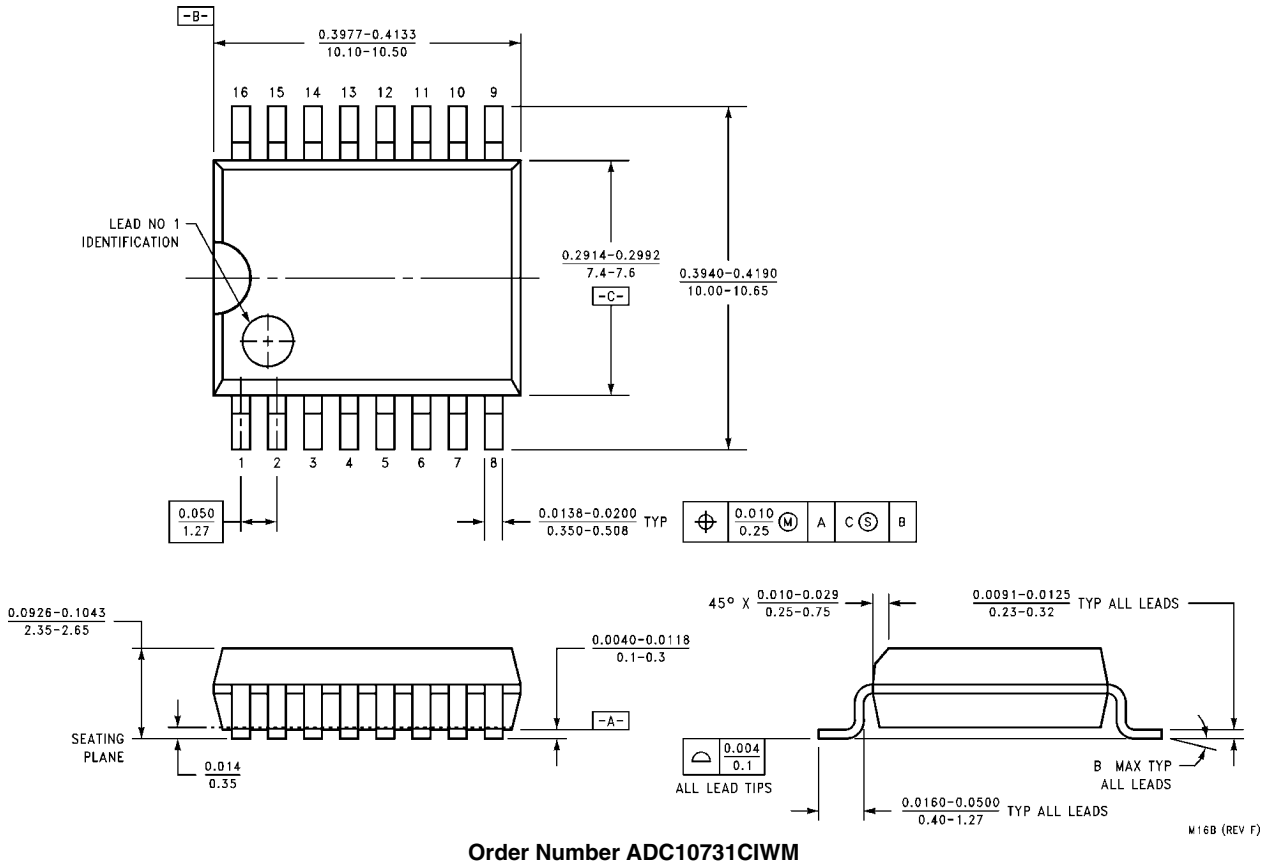
FIGURE 17. Protecting the Analog Inputs



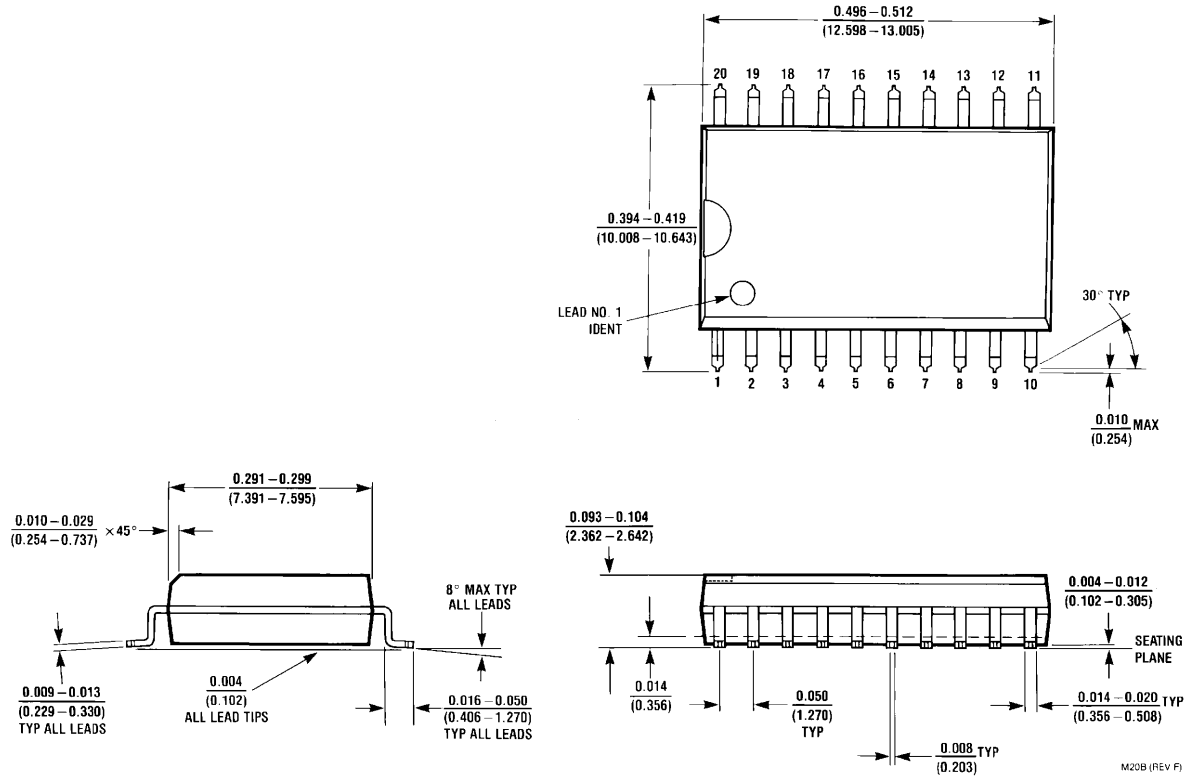
*1% resistors

FIGURE 18. Zero-Shift and Span-Adjust for Signed or Unsigned, Single-Ended Multiplexer Assignment, Signed Analog Input Range of 0.5V ≤ V_{IN} ≤ 4.5V

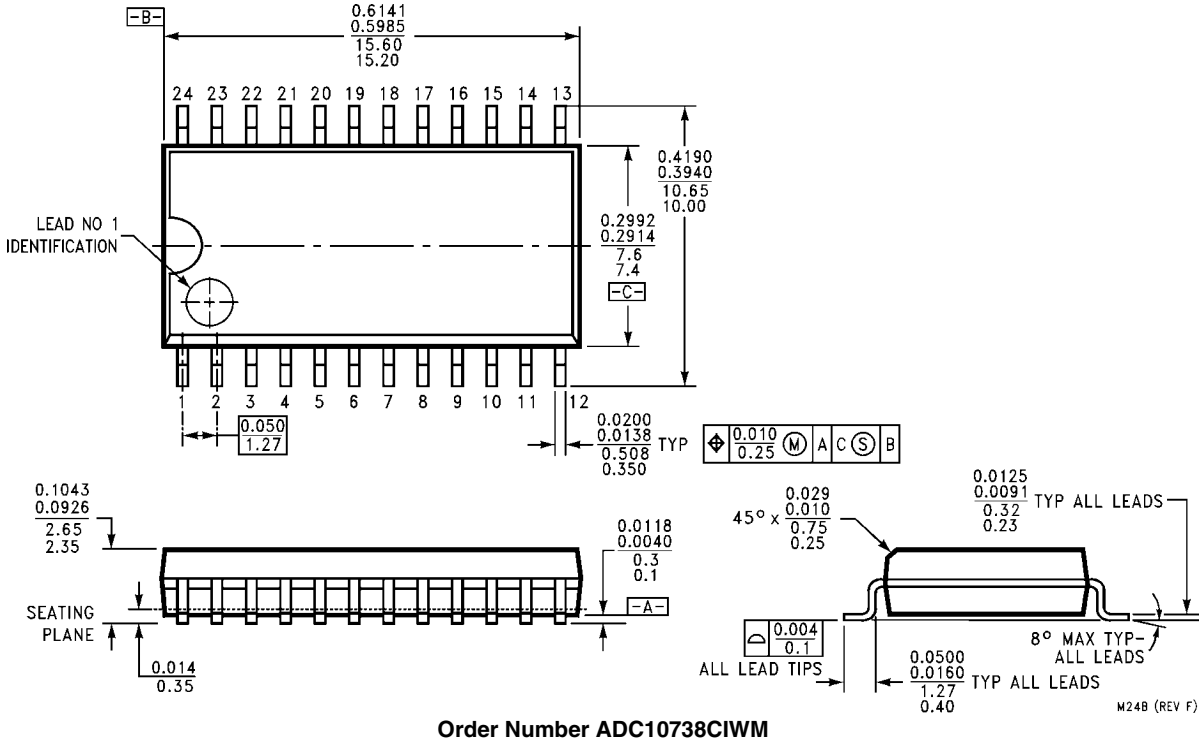
Physical Dimensions inches (millimeters) unless otherwise noted



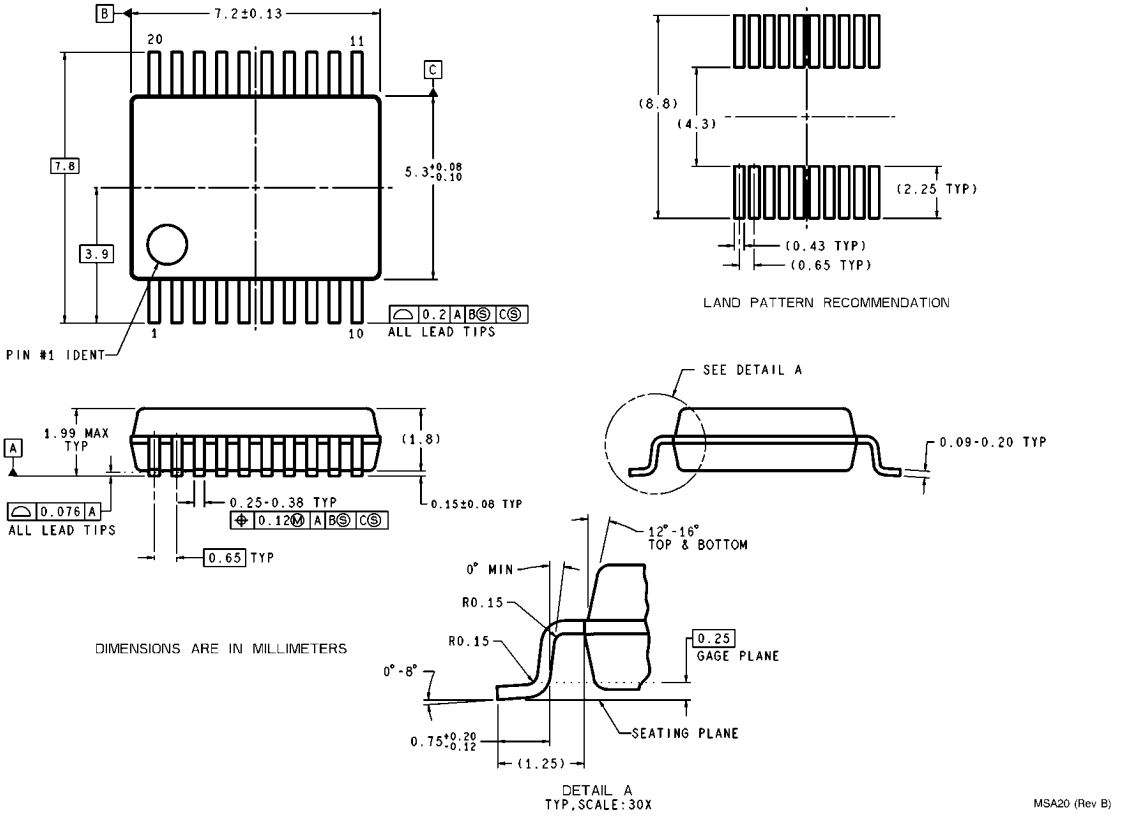
Order Number ADC10731CIWM
NS Package Number M16B



Order Number ADC10732CIWM and ADC10734CIWM
NS Package Number M20B



Order Number ADC10738CIWM
NS Package Number M24B



Order Number ADC10734CIMSA
NS Package Number MSA20

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